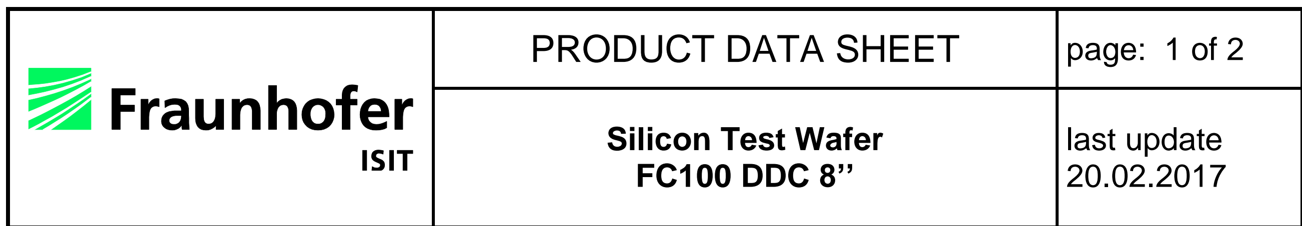
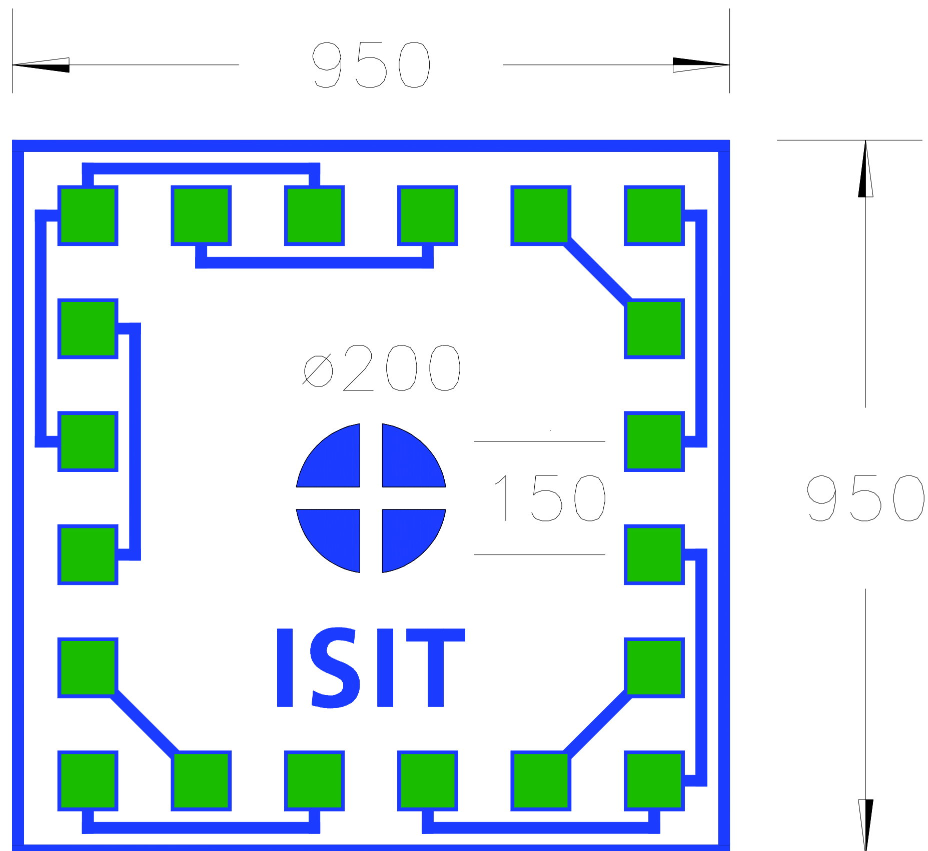
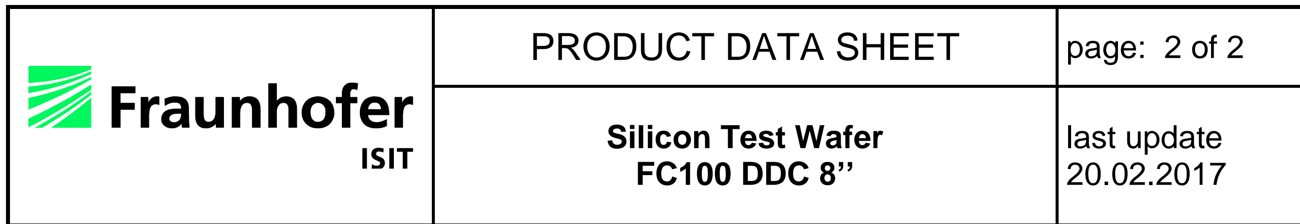


LAYOUT:



TECHNICAL DATA:

- Flip Chip Silicon Die
- dummy component with two nested daisy chains, allowing
  - easy measurement of short cuts between adjacent contacts
  - advanced reliability tests with voltage applied between adjacent pads
- 2 Kelvin sensing structures for 4-point probe contact resistance measurement
- fiducial mark for automated placement
- design size 0.95 mm x 0.95 mm with 50 µm dicing street
- aluminium pads 80 µm x 80 µm
- passivation opening 70 µm x 70 µm
- contact pitch 150 µm
- custom specific wafer thickness
- pad modifications with electroless NiAu and stud bumps available



TECHNICAL INFORMATION:

designed chip size	0.95 mm x 0.95 mm
die pitch	1.00 mm x 1.00 mm
typical die size after dicing	0.97 mm x 0.97 mm other geometries, e.g. 4x4 dies available on request
wafer thickness	300 µm, other thicknesses available on request
pad layout	20 pads, two nested daisy chains with 150µm pitch and 2 Kelvin sensing structures for contact resistance measurement
pad geometry	aluminum: 80µm x 80µm (square) passivation opening: 70µm x 70µm (square)
pad metal	1.4 µm AlCu0.5
passivation	PECVD: 300 nm LTO + 800 nm SiN
optional pad modifications	electroless NiAu and stud bumps
delivery	8” wafer, 25800 dies, diced on tape
normal uses	High throughput die and flip chip placing from wafer feeder, automatic wire bonding, encapsulation and underfill processes. Reliability tests with voltage applied between adjacent pads.
typical technologies	• wire bonding • stud-bump bonding • anisotropic conductive adhesive flip chip (ACA / ESC5) • isotropic conductive adhesive flip chip (ICA)
available substrates	Substrates may be designed on request
contact	Fraunhofer Institut Siliziumtechnologie Fraunhoferstraße 1; D-25524 Itzehoe Internet: http://www.isit.fraunhofer.de Dr.-Ing. Dipl. Phys. Dirk Kähler Phone +49 (0) 48 21 / 17 – 46 04 Fax +49 (0) 48 21 / 17 – 42 50 Email: dirk.kaehler@isit.fraunhofer.de Dr.-Ing. Wolfgang Reinert Phone +49 (0) 48 21 / 17 – 42 16 Fax +49 (0) 48 21 / 17 – 42 50 Email: wolfgang.reinert@isit.fraunhofer.de
geometry variations	Arbitrary customer-specific layouts including a company's logotype can be realised on 8” glass and silicon wafers.

* Specifications subject to change without notice.